YHM8211A

Brushed DC Motor Driver with Internal Current Sense

Preliminary

Features

- N-channel H-bridge brushed DC motor driver.
- 2.8V to 9V operating supply voltage range.
- 400mΩ R_{ON} NMOS with internal mirror current sense.
- High output current capability: 4.1A Peak
- PWM control interface
- Supports 1.8V, 3.3V, and 5V logic inputs
- Integrated ISNS current sensing for stall detection and current regulation
- Low-power sleep mode
  - <1μA at V_{DD} = 9V, T_J = 25°C
- Integrated protection features
  - VDD undervoltage lockout (UVLO)
  - Auto-retry overcurrent protection (OCP)
  - Thermal shutdown
- Package:
  - YHM8211A: 8-Pin DFN

Applications

- Vacuum Robot
- Printer

General Description

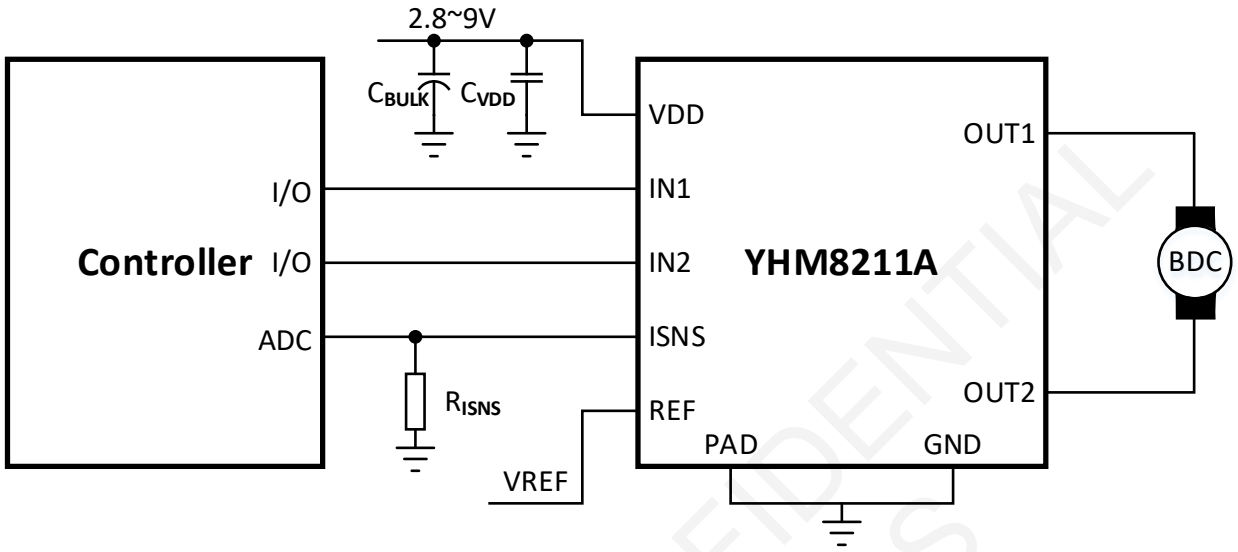
The YHM8211A is a motor driver for brushed DC motor application. It is integrated H-bridge MOSFET with very low R_{ON}. Internal charge pump improves efficiency by supporting N-Channel MOSFET half bridges and 100% duty cycle driving. One current sense/regulation and various protection functions circuits are integrated in the device.

For YHM8211A, an internal current mirror architecture on the ISNS pin implements current sensing and regulation. This eliminates the need for a large power shunt resistor, saving board area and reducing system cost. The Microcontroller's ADC can measure voltage on ISNS pin to detect motor stall or changes in load conditions. The external voltage reference pin, REF, determines the threshold of current regulation during start-up and stall events without interaction from a microcontroller.

YHM8211A can enter sleep mode to save power consumption by shutting down most of the internal circuit. Internal protection features include UVLO, OCP and OTP.

YHM8211A are available in 8-PIN DFN. It operates over an ambient temperature range from -40°C to +125°C.

Typical Application



Internal Block Diagram

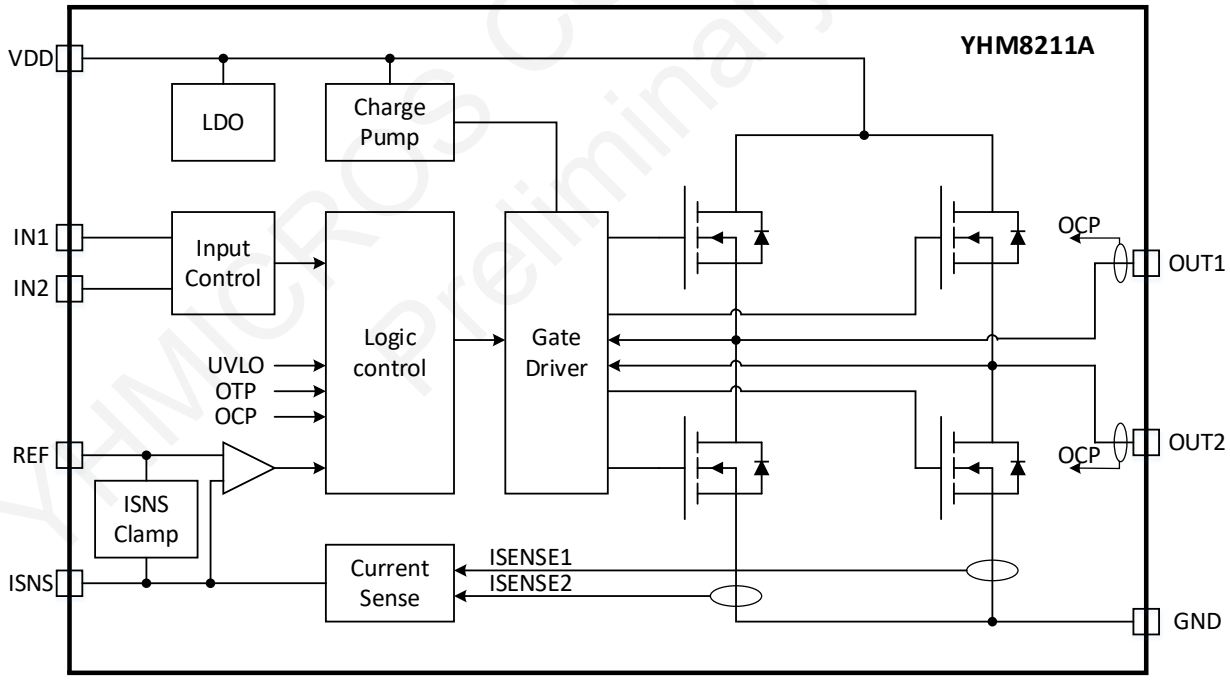


Figure 1. YHM8211A Functional Block Diagram

Pin Configurations

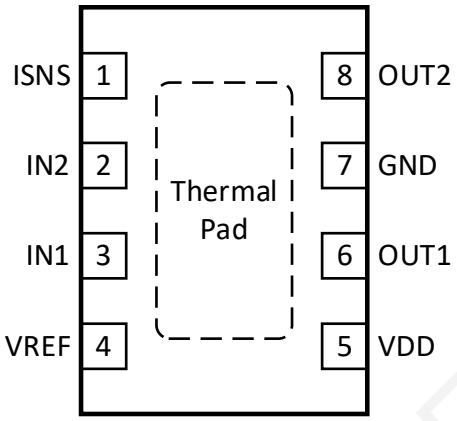


Figure 2. YHM8211A DFN-8 Pin Assignment (Top View)

YHM8211A Pin Descriptions

Pin	Name	Description
1	ISNS	Current output proportional to low side MOSFET load current.
2	IN2	H-bridge output control signal input 2. Pulled down internally.
3	IN1	H-bridge output control signal input 1. Pulled down internally.
4	REF	Voltage input for output current regulation threshold setting.
5	VDD	Power supply. Connect 0.1μF bypass capacitor to GND
6	OUT1	H-bridge output 1. Connect to Motor directly.
7	GND	Device power ground.
8	OUT2	H-bridge output 2. Connect to Motor directly.
	PAD	Thermal pad. Connect to GND on board.

1 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	VDD to GND		-0.3	16	V
V_{OUT}	OUT to GND		-0.7	V_{IN}+0.7	V
V_{IN}	IN to GND		-0.3	6	V
V_{ISNS}	ISNS to GND		-0.3	6	V
V_{REF}	REF to GND		-0.3	6	V
I_{OUT}	Output Current (Continuous)		Internal Limited	Internal Limited	A
T_{STG}	Storage Temperature Range		-65	150	°C
T_J	Junction Temperature		-40	150	°C
T_A	Ambient Temperature		-40	125	°C
θ_{JA}	Thermal Resistance, Junction-to-Ambient (1-in. Pad of 2-oz. Copper)			TBD	°C/W
ESD	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	±2		KV
	Charged Device Model, JESD22-C101	All Pins	±0.75		

Note 1. Refer to JEDEC JESD51-7, use a 4-layerboard

2 Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance.

Parameters	Min.	Max.	Unit
Input Voltage: V_{DD}	2.8	9	V
Peak Output Current: I_{SNS}	0	3	mA
Logic Input Voltage: V_{IN}	0	5.5	V
Reference Voltage: V_{REF}	0	3.6	V
PWM input frequency: f_{PWM}	0	200	KHz
Output Current: I_{OUT}	0	4.1	A
Ambient Temperature Range	-40	125	°C
Operating Junction Temperature Range	-40	150	°C

3 Thermal Information

Symbol	Parameter	Min.	Max.	Unit
P_D	Total Power Dissipation at TA = 25°C		TBD	W
θ_{JA}	Thermal Resistance, Junction-to-Ambient (1-in. Pad of 2-oz. Copper)		TBD	°C/W
θ_{JC}	Thermal Resistance, Junction-to-Case		TBD	°C/W

4 Electrical Characteristics

Condition: 4.5V < V_{DD} < 24V, T_A = - 40°C ~ 125°C, unless otherwise noted. Typical value at T_A = 25°C and V_{DD} = 9V.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range	V_{DD}		2.8		9	V
Under Voltage Lockout	V_{UVLO}	V_{DD} rising		2.7	2.75	V
Under Voltage Lockout Hysteresis	V_{UVLO_HYS}			100		mV
UVLO debounce Time	t_{UVLO}			10		μs
Wake up Time	t_{WAKE}	IN signal from 0 to 1.			250	μs
Turn off Time	t_{SLEEP}	IN signal from 1 to 0	0.8		1.5	ms
Operating Power Supply Current	I_{DDQ}	IN1=IN2=1;		0.4	1	mA
Input Power Current in Sleep Mode	I_{DD}	IN1=IN2=0;			1.3	μA
IN Logic Voltage	V_{IH}		1.5			V
	V_{IL}				0.5	
Input Voltage Hysteresis	V_{HYS}			200		mV
IN Pull Down Resistor	R_{PD}	V_{IN} = 3.3V		100		KΩ
High Side Switch on Resistance	R_{ON_HS}	V_{DD} = 9V, I_{OUT} =1 A, f_{PWM} = 25KHz		220		mΩ
Low Side Switch on Resistance	R_{ON_LS}	V_{DD} = 9V, I_{OUT} =1 A, f_{PWM} = 25KHz		220		mΩ
Body Diode Forward Voltage	V_F	I_{OUT} =1 A		0.8		V
Output Rising Time	t_{RISE}	VDD = 9V, OUTx from 10% to 90%		220		ns

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Falling Time	t_{FALL}	VDD = 9V, OUTx from 90% to 10%		220		ns
IN to OUT Propagation Time	t_{PG}			0.7	1	μs
Output Dead Time	t_{DEAD}			200		ns
ISNS Current Mirror Scaling Factor	A_{ISNS}			1575		μA/A
Current Mirror Error	A_{EER}	I_{OUT} =1.5 A, V_{DD} > 6.5V, V_{SNS} < 3V.	-5		5	%
Current Regulation off Time	t_{OFF}			25		μs
Current Regulation Blanking Time	t_{BLK}			1.4		μs
Current Sense Delay Time	t_{DELAY}			1.1		μs
Current Regulation Debounce Time	t_{DEB}			0.7		μs
OCP Threshold	I_{OCP}		4.1			A
OCP Response Time	t_{OCP}			1.5		μs
OCP Retry Time	t_{RETRY}			3		ms
Thermal Shutdown Threshold	T_{SD}		150	160		°C
Thermal Hysteresis	T_{HYS}			30		°C

5 Timing Diagram

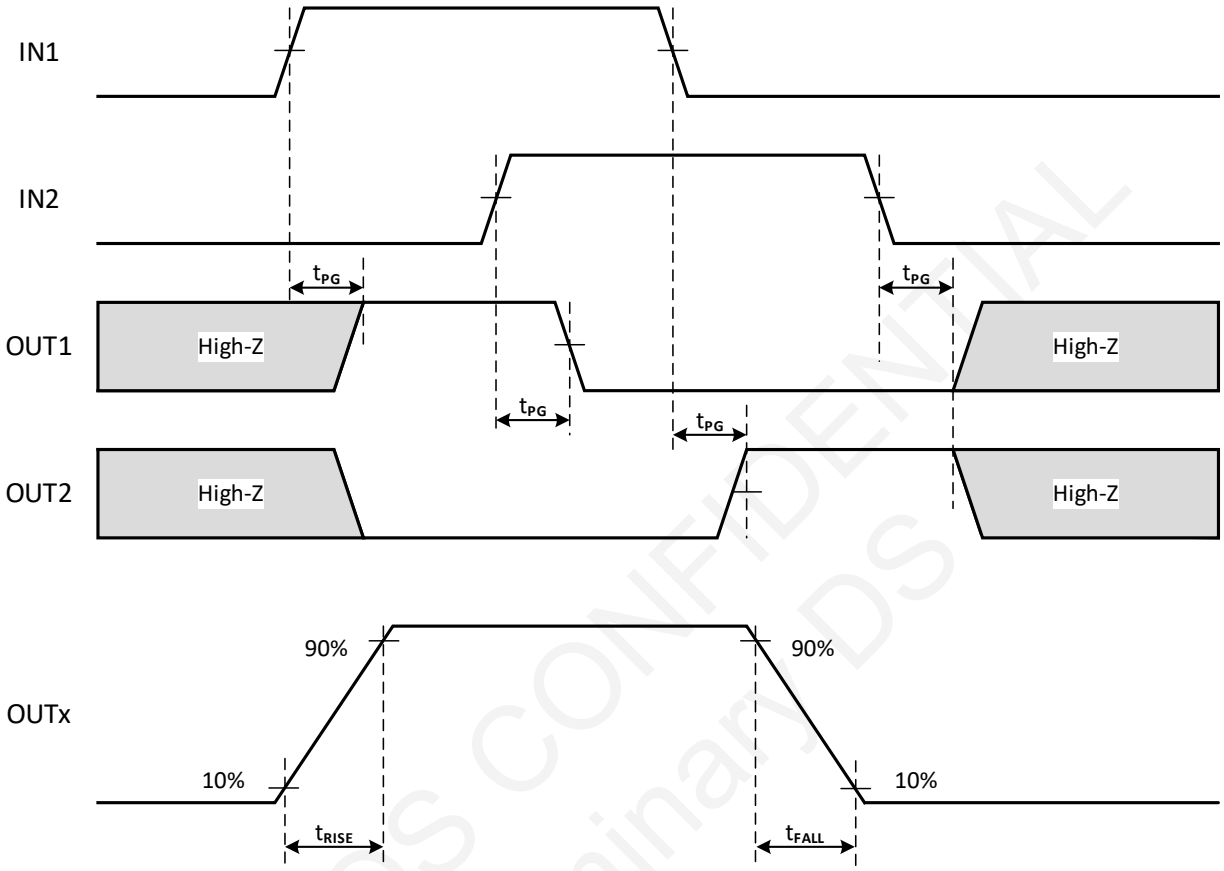


Figure 3. IN to out timing diagram

6 Typical Operating Characteristics

TBD

7 Detailed Description

7.1 General Introduction

YHM8211A is designed for driving brushed DC motors. Two logic inputs(INx) control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical R_{ON} of 440 mΩ (including one high-side and one low-side FET). VDD is device's power supply and its range is from 4.5V to 9V. It is used for both device internal circuit and motor winding bias voltage. The integrated charge pump of the device boosts VDD internally and fully drive the high-side N-channel MOSFETs. Motor speed can be controlled with pulse-width modulation at frequencies between 0 to 200 kHz. The device enters a low-power sleep mode by bringing both inputs low.

YHM8211A integrates current mirror circuit. The ISNS pin sources a small current that is proportional current to low-side power MOSFETs current. With external R_{ISNS}, microcontroller ADC can measure this current and finally calculate the current flows in motor. This circuit can remove traditional external shunt resistor to save system cost.

These integrated current regulation features allow the device to limit the output current with a fixed off-time PWM chopping scheme. The REF pin configures the current regulation level during motor operation to limit the load current.

A variety of integrated protection features protect the device in the case of a system fault. They include UVLO, OCP and thermal shutdown.

7.2 Bridge Control

YHM8211A output consists of four N-channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in Table 1.

IN1	IN2	OUT1	OUT2	Description
0	0	High-Z	High-Z	Coast: H-Bridge disable. Enter sleep mode after 1ms.
0	1	L	H	Reverse Driving. Current direction: OUT2 → OUT1.
1	0	H	L	Forward Driving. Current direction: OUT1 → OUT2.
1	1	L	L	Braking: low side slow decay.

Table 1 H-Bridge Control

The inputs (INx) can be set to static voltages for 100% duty cycle drive. or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, H-bridge is switching between driving and braking mode. For example, to drive a motor forward with 50% PWM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for fast current decay is also available. Figure 5 shows how the motor current flows through the H-bridge. The input pins can be powered before VDD is applied.

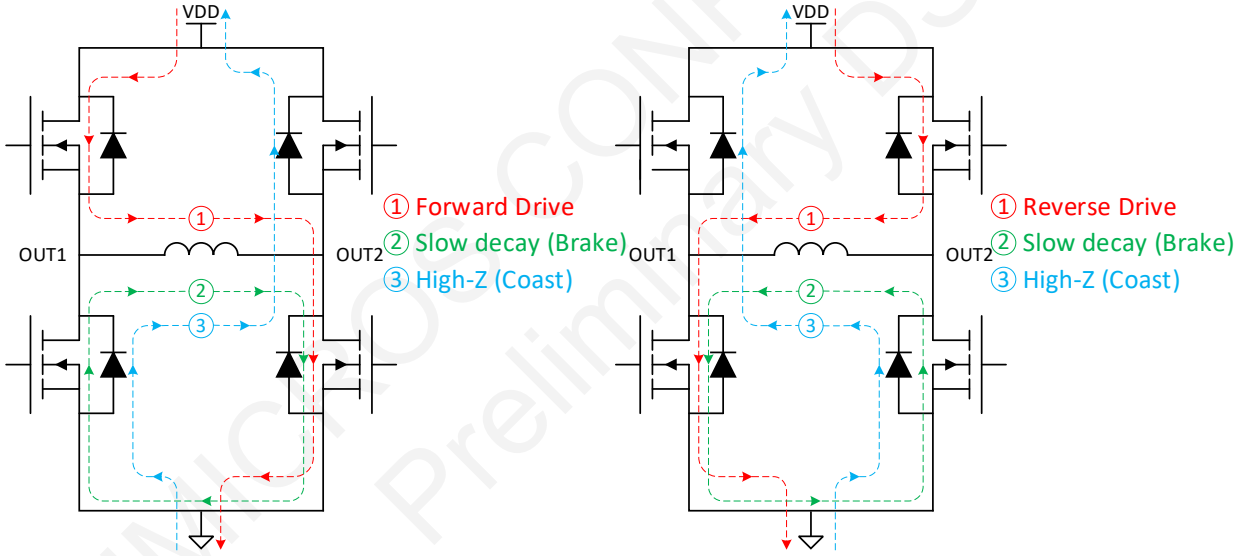


Figure 4. H-Bridge Current Path

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. During t_{DEAD} time, the output is High-Z. The OUTx voltage depends on the direction of current during this time. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above VDD. This diode is the body diode of the high-side or low-side FET. The propagation delay time (t_{PG}) is measured as the time between an input edge to output change. This time includes input debounce time and other internal logic propagation delays. The input debounce time prevents noise on the input pins from affecting the output state. Additional output slew delay timing accounts for FET turn on or turn off times (t_{RISE} and t_{FALL}). Figure 6 below shows the timing of the inputs and outputs of the motor driver.

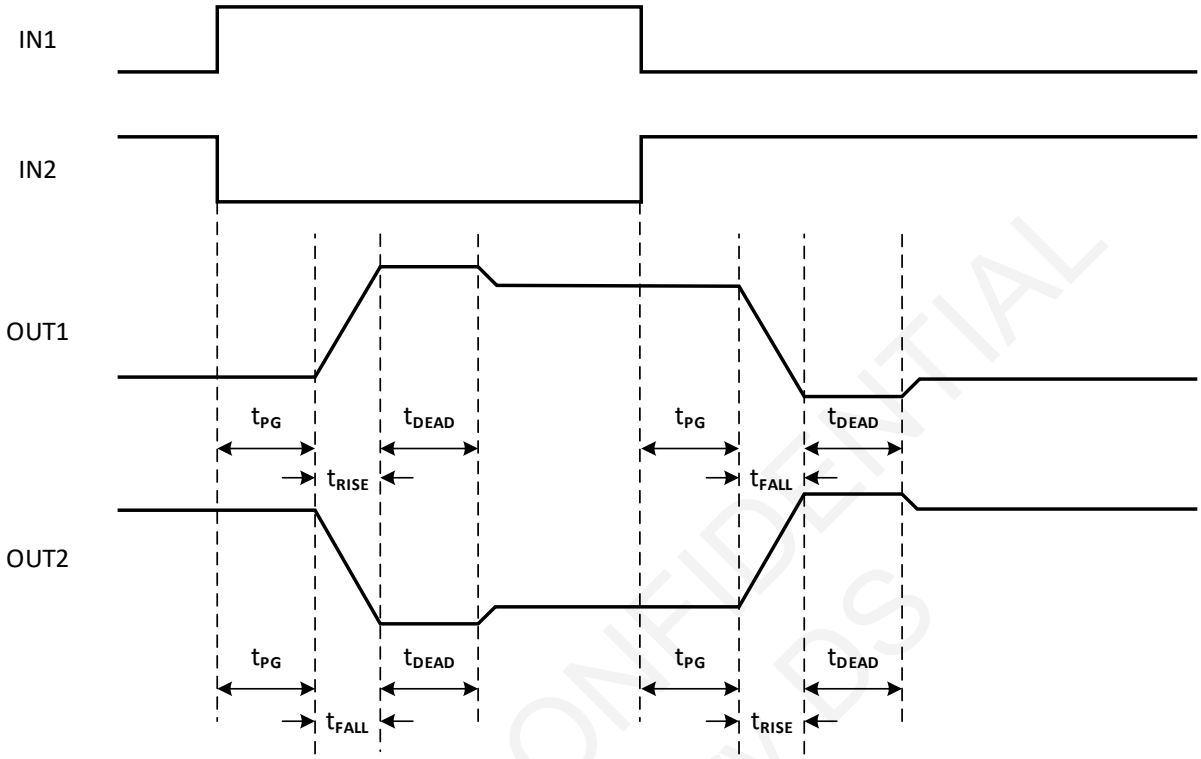


Figure 5. H-Bridge Timing Diagram

7.3 Current Sense and Regulation

YHM8211A device integrates current sensing and regulation feature. These features allow the device to sense the output current without an external sense resistor or sense circuitry reducing system size, cost, and complexity. This also allows for the device to limit the output current in the case of motor stall or high torque events and give detailed feedback to the controller about the load current through a current proportional output. Figure 7 shows the ISNS timings specified in the Electrical Characteristics table.

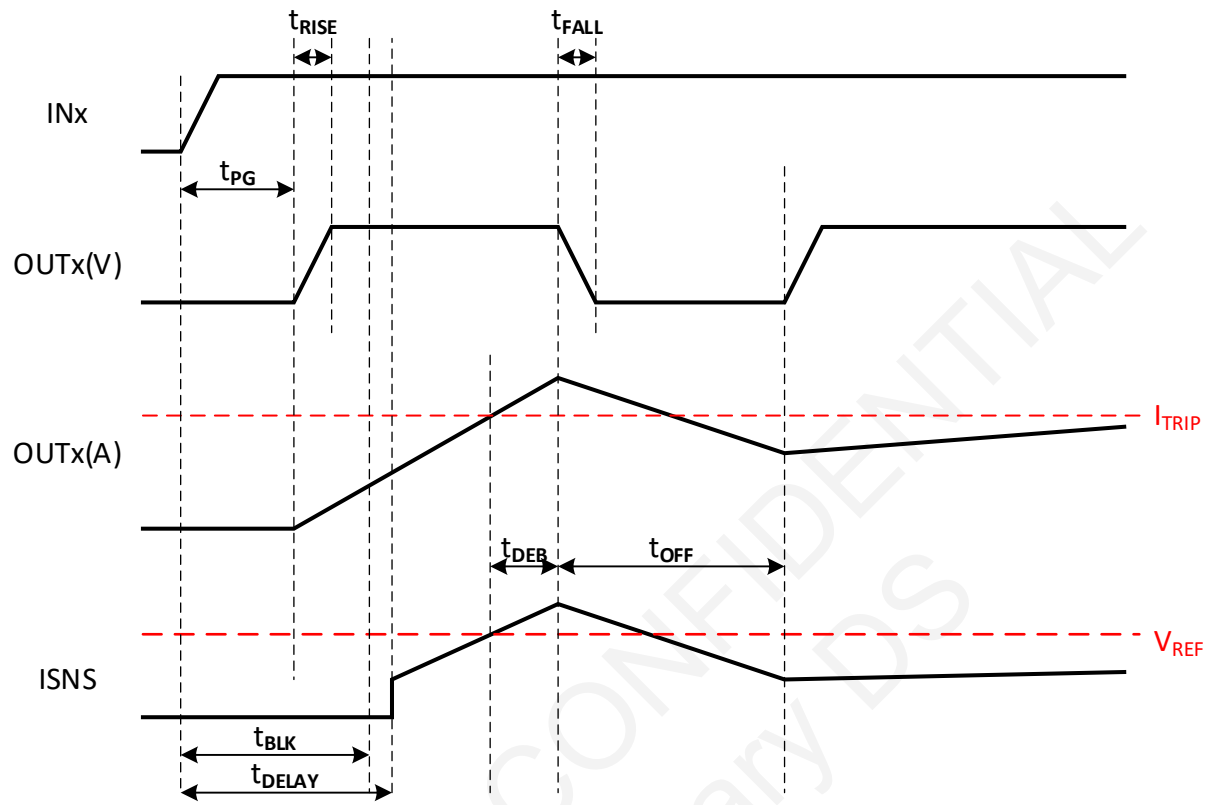


Figure 6 ISNS Timing Diagram

7.3.1 Current Sense

The ISNS pin output is an analog current. It is proportional to the sum of current flowing through both the low-side MOSFETs in the H-bridge. The factor is A_{ISNS}. The ISNS output current can be calculated by Equation 1. The I_{LSx} in Equation 1 is only valid when the current flows from drain to source in the low-side MOSFET. If current flows from source to drain or through the body diode, the value of I_{LSx} for that channel is zero. So, if the bridge is in the brake, slow-decay state, then the current out of ISNS is only proportional to the current in one of the low-side MOSFETs.

$$\boldsymbol{I_{ISNS}\,(\mu A) = (I_{LS1} + I_{LS2})(A) \times A_{ISNS}\,(\mu A/A)} \quad (1)$$

The A_{ERR} parameter in the Electrical Characteristics table is the total error for A_{ISNS} gain. It includes the effect of offset error and gain error.

The motor current can be measured by an internal current mirror on both low side MOSFETs. This architecture can remove traditional external sense resistor to reduce system power lost. The current mirror architecture can continuously measure motor winding current in both drive and brake period in typical bidirectional brushed DC motor applications. In coast mode, the current is freewheeling and cannot be sensed because it flows from source to drain. The ISNS pin should be connected to an external resistor (R_{ISNS}) to ground to generate a voltage (V_{ISNS}) on the ISNS pin with the analog current output. This allows system to get motor current data with a standard analog to digital converter (ADC). The R_{ISNS} resistor can be changed based on the expected load current in the application so that the full range of the controller ADC is utilized. Additionally, YHM8211A has an internal voltage clamp circuit between REF and ISNS to protect the external ADC input in case of overcurrent or unexpected high current events. V_{ISNS} is limited with respect to V_{REF} on the REF pin. The corresponding ISNS voltage to the output current can be calculated by Equation 2.

$$V_{ISNS}\,(V) = I_{ISNS}\,(A) \times R_{ISNS}\,(\Omega) \quad (2)$$

The ISNS output bandwidth is limited by the sense delay time (t_{DELAY}) of the internal current sensing circuit. This time

is the delay from the low-side MOSFET enable command (from the INx pins) to the ISNS output being ready. But if the device is alternating between drive and slow decay (brake) in an PWM pattern then current sense circuit is continuously on and the sense delay time has no impact to the ISNS output. If a command on the INx pins disables the low-side MOSFETs (according to the logic tables in Section 1.2), the ISNS output will disable with the input logic signal. Although the low-side MOSFETs may still conduct current as they disable according to the device slew rate (noted in the Electrical Characteristics table by t_{RISE} time), ISNS will not represent the current in the low-side MOSFETs during this turnoff time.

7.3.2 Current Regulation

YHM8211A integrates current regulation using a fixed off-time current chopping scheme. This allows the devices to limit the output current in case of motor stall, high torque, or other high current load events without involvement from the external controller as shown in Figure 8.

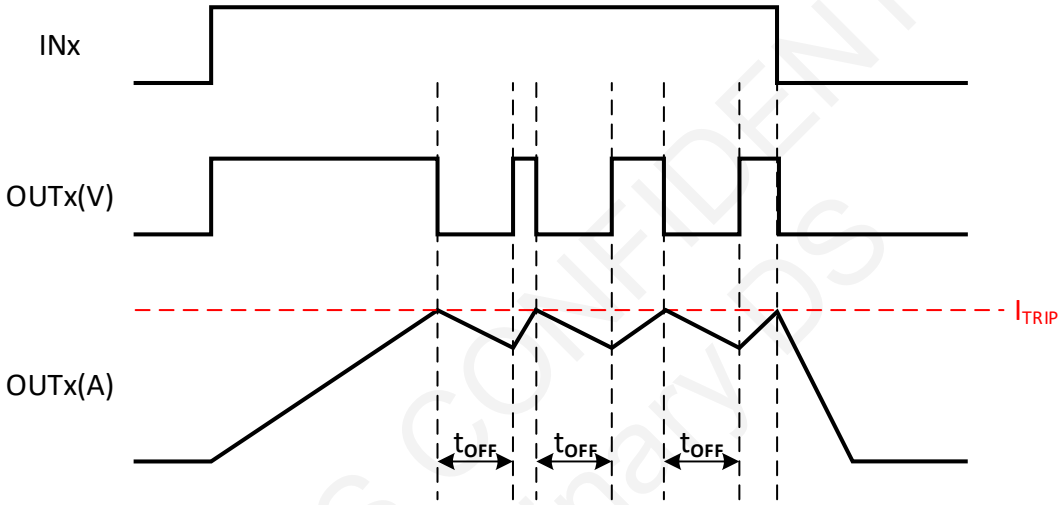


Figure 7. Current Regulation Action

The current regulation threshold (I_{TRIP}) is calculated by Equation 3.

$$I_{TRIP}(A) \times A_{ISNS}(\mu A/A) = \left(V_{REF}(V)/R_{ISNS}(\Omega)\right) \times 10^6 \quad (3)$$

There, V_{REF} is voltage on REF pin and R_{ISNS} is resistor on ISNS pin.

For example, if V_{REF} = 3.3 V, R_{ISNS} = 1048Ω and A_{ISNS} = 1575 μA/A, then I_{TRIP} will be about 2A.

The fixed off-time current regulation scheme supports up to 100% duty cycle current regulation since the H-bridge automatically enables after the t_{OFF} period and does not require a new control input edge on the INx pins to reset the outputs. When the motor current exceeds the I_{TRIP} threshold, the outputs will enter a current regulation mode with a fixed off time (t_{OFF}). After this time, H-bridge automatically enables. This means it does not need new control signal on INx to reset output. So, this scheme supports up to 100% duty cycle current regulation. During t_{OFF}, the H-bridge enters a brake state, the outputs re-enable according to the control inputs if I_{OUT} is less than I_{TRIP}. Otherwise, the H-bridge enters another brake status for t_{OFF}. If the state of the INx control pins changes during the t_{OFF} time, the remainder of the t_{OFF} time is ignored, and the outputs will follow the inputs. The I_{TRIP} comparator has both a blanking time (t_{BLK}) and a debounce time (t_{DEB}) to avoid the effect of external voltage and current transient events. These events may be caused by capacitors inside motor or motor connections. If the internal debounce time is not enough, one small value capacitor can be placed on ISNS pin. The value needs to change in different application and large capacitor may slow down the response time of current regulation circuit. All the effort which used is to prevent transient condition to prematurely trigger the current regulation. The internal current regulation and current sense function can be disabled by tying ISNS to GND and setting the REF pin voltage greater than GND. If current sense function is required but current regulation is not required, changing V_{REF} and R_{ISNS} and making sure V_{ISNS} always lower than V_{REF}. V_{REF} range need match recommended operation conditions table.

7.4 UVLO (Under-Voltage Lockout)

The device has a built-in under-voltage lockout (UVLO) circuit to monitor VDD supply. When V_{VDD} is rising, the output remains disabled until VDD voltage is above 2.7V (TYP). This circuit has a 100mV hysteresis to provide noise immunity to transient conditions. When VDD voltage drop below V_{UVLO}-V_{UVLO_HYS}, all internal circuits are disabled, all output MOSFETs are disabled and logic circuit is reset.

7.5 OCP (Over Current Protection)

Current limit circuit is designed on each MOSFET. If current which flows through any of these FETs higher than OCP threshold for t_{OCP}, all MOSFETs turn off. After t_{RETRY}, YHM8211A re-enables FETs according to INx setting. If the fault condition is still present, the device enters OCP mode and repeat these actions. Over current conditions are independently detected on each low-side or high-side MOSFET. This means it can detect all the over current conditions, such as short to GND, short to VDD or motor winding overcurrent. All these conditions can cause OCP action. OCP detection is independent from current sense and current regulation circuit.

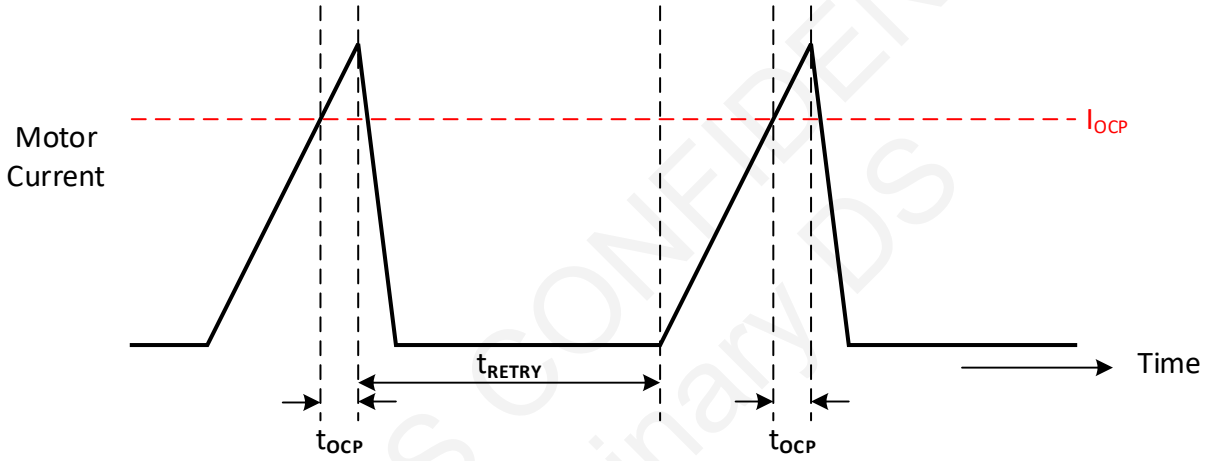


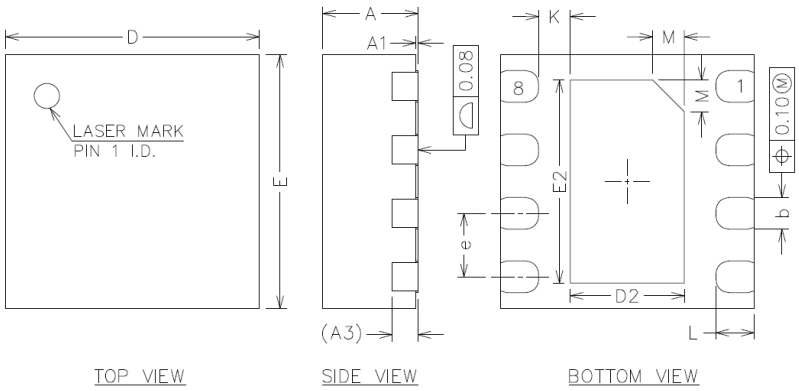
Figure 8. OCP Operation

7.6 Thermal Shutdown

YHM8211A has a thermal shutdown function. When the junction temperature exceeds T_{SD}, all MOSFETs are disabled. The device exits thermal shutdown and operation resume after junction temperature cools down below T_{SD}-T_{HYS}.

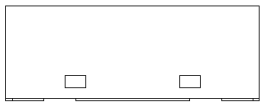
8 Package Dimensions

DFN-8



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.80	0.90	1.00
E2	1.50	1.60	1.70
e	0.40	0.50	0.60
K	0.15	0.25	0.35
L	0.25	0.30	0.35
M		0.25REF	



SIDE VIEW

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-229
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

9 Ordering Information

Part Number	Temp Range	Pin Package	Top Mark	MOQ
YHM8211AD8T	-40°C to 125°C	8 DFN	YH8211A	4000

T = Tape and reel.

Datasheet Change History

Rev	Date	Changes
0.0	Oct/2023	Initial Version