YHM4208

8-Bits Auto-Bidirectional Voltage Level Translators

V1.01 Preliminary

Features

- V_{CC} Range:
  - V_{CCA}: 1.2V to 5.5V
  - V_{CCB}: 1.65V to 5.5V
- Maximum Data Rate:
  - Push Pull: 100Mbps
  - Open Drain: 1.1Mbps
- Support V_{CC} isolation function.
- Ultra-Low I_Q On Each V_{CC}: 5μA
- OE referenced to V_{CCA}.
- Support Partial Power Down Mode.
- Working Temperature Range: - 40°C to + 85°C
- Package:
  - 20-Pin 3.5mm x 4.5mm VQFN20
  - 20-Pin 3mm x 3mm QFN20
  - 20-Pin 6.5mm x 4.4mm TSSOP20

Applications

- Portable device
- GPIO
- I2C/SMBUS
- UART/SPI

General Description

The YHM4208 is an auto-bidirectional voltage level translators family to support 8 bits applications. These device A port tracks the V_{CCA} voltages and its range is from 1.2V to 5.5V. B port tracks the V_{CCB} voltages and its range is from 1.65V to 5.5V.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance (Hi-Z) state. And if either one of V_{CC} is absent and pull to GND, the outputs are also placed in Hi-Z state. And OE input circuit is reference to V_{CCA}. To ensure the Hi-Z state during power-up or power-down periods, tie OE to GND through a pull-down resistor.

The YHM4208 is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The YHM4208 operates over an ambient temperature range of - 40°C to + 85°C.

Typical Application

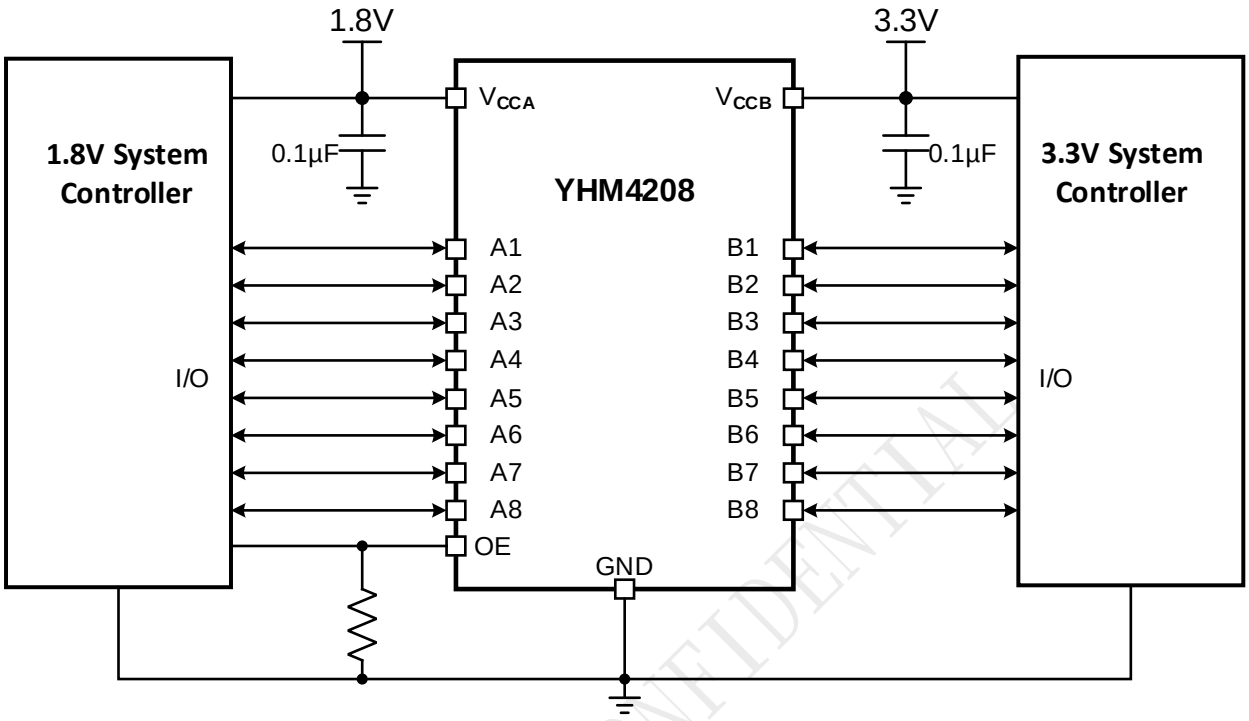


Figure 1. YHM4208 Application Diagram

Pin Configurations

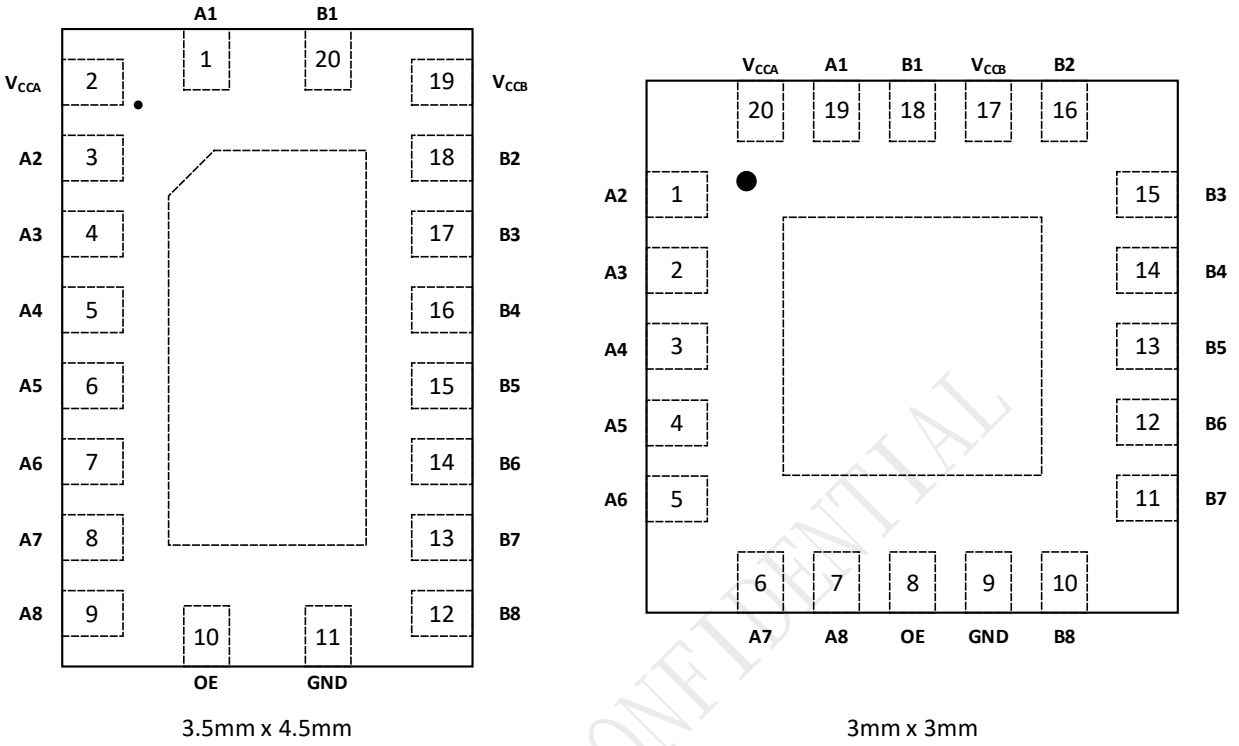


Figure 2. YHM4208 QFN-20 Pin Assignment. (Top View)

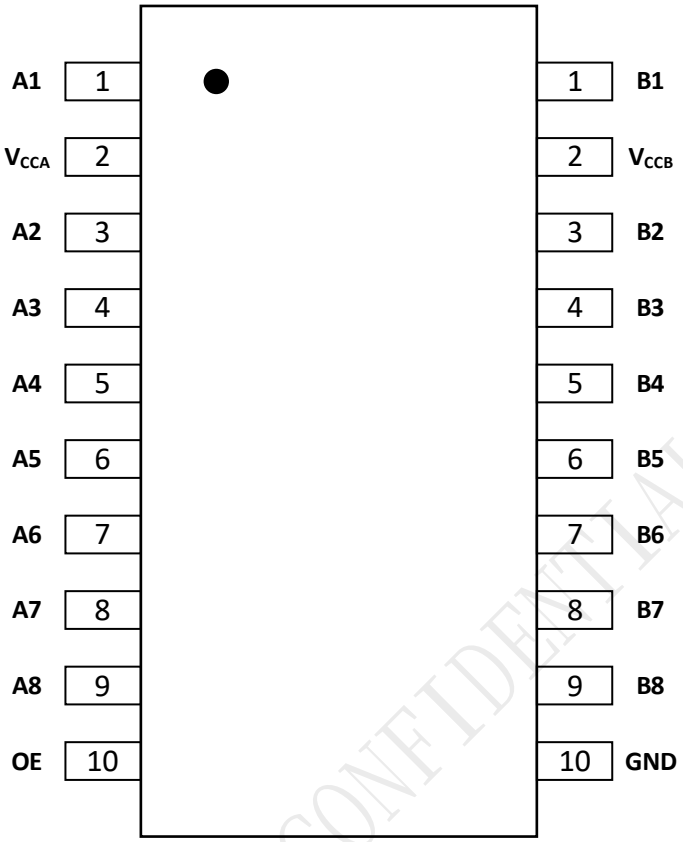


Figure 3. YHM4208 TSSOP-20 Pin Assignment. (Top View)

YHM4208 Pin Descriptions

VQFN (3.5mm x 4.5mm) TSSOP	QFN (3mm x 3mm)	Name	Description
1	19	A1	Input/output 1. Referenced to V_{CCA}
2	20	V_{CCA}	A port power supply. 1.2V ≤ V_{CCA} ≤ 5.5V
3	1	A2	Input/output 2. Referenced to V_{CCA}
4	2	A3	Input/output 3. Referenced to V_{CCA}
5	3	A4	Input/output 4. Referenced to V_{CCA}
6	4	A5	Input/output 5. Referenced to V_{CCA}
7	5	A6	Input/output 6. Referenced to V_{CCA}
8	6	A7	Input/output 7. Referenced to V_{CCA}
9	7	A8	Input/output 8. Referenced to V_{CCA}
10	8	OE	Output enable pin. Active high. Pull OE low to place all outputs in tri-state mode. Referenced to V_{CCA}.
11	9	GND	Ground
12	10	B8	Input/output 8. Referenced to V_{CCB}
13	11	B7	Input/output 7. Referenced to V_{CCB}
14	12	B6	Input/output 6. Referenced to V_{CCB}

VQFN (3.5mm x 4.5mm) TSSOP	QFN (3mm x 3mm)	Name	Description
15	13	B5	Input/output 5. Referenced to V_{CCB}
16	14	B4	Input/output 4. Referenced to V_{CCB}
17	15	B3	Input/output 3. Referenced to V_{CCB}
18	16	B2	Input/output 2. Referenced to V_{CCB}
19	17	V_{CCB}	B port power supply. 1.65V ≤ V_{CCB} ≤ 5.5V and V_{CCA} ≤ V_{CCB}
20	18	B1	Input/output 1. Referenced to V_{CCB}

1 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CCA}, V_{CCB}	V_{CCA}, V_{CCB} to GND		-0.3	6	V
V_I	Input Voltage Range, Port A, Port B		-0.3	6	V
V_O	Output Voltage Range for the High-Impendence or Power Off States, Port A, Port B.		-0.3	6	V
V_O	Output Voltage Range for the High or Low States, Port A		-0.3	V_{CCA}	V
V_O	Output Voltage Range for the High or Low States, Port B		-0.3	V_{CCB}	V
I_{IK}	Input Clamp Current, $V_I < 0$			50	mA
I_{OK}	Output Clamp Current, $V_O < 0$			-50	mA
I_C	Continuous Current through V_{CCA}, V_{CCB}, or GND		-100	100	mA
T_J	Maximum Junction Temperature			+150	°C
ESD	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	5		KV
		Port B	13		
	Charged Device Model, JESD22-C101	All Pins	2		

Note 1. Refer to JEDEC JESD51-7, use a 4-layerboard.

2 Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance.

Parameters		Min.	Max.	Unit
Voltage Supply: V_{CCA}		1.2	5.5	V
Voltage Supply: V_{CCB}		1.65	5.5	V
High Level Input Voltage: V_{IH} (Note 1)	Data Port	0.85 x V_{CCI}	V_{CCI}	V
	OE	0.85 x V_{CCA}	5.5	V
Low Level Input Voltage: V_{IL} (Note 1)	Data Port	0	0.15	V
	OE	0	0.15	V
Input Transition Rise or Fall Rate: Δt/ΔV	A Port (Push-Pull)		10	ns/V
	B Port (Push-Pull)		10	ns/V
Operating Ambient Temperature Range		-40	85	°C

3 Electrical Characteristics

Condition: T_A = -40°C to +85°C. Typical values are at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Port A Output High Voltage	V_{OHA}	I_{OH} = -20μA, T_A = 25°C, $V_{IB} \geq V_{CCB}$ - 0.4V	0.9* V_{CCA}			V
Port A Output Low Voltage	V_{OLA}	V_{CCA} = 3V, V_{CCB} = 3.3V. I_{OL} = 400μA, T_A = 25°C, $V_{IB} \leq$ 0.15V			0.55	V
Port B Output High Voltage	V_{OHB}	I_{OH} = -20μA, T_A = 25°C, $V_{IA} \geq V_{CCA}$-0.2V	0.9* V_{CCB}			V

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Port B Output Low Voltage	V_{OLB}	V_{CCA} = 3.3V, V_{CCB} = 4.5V. I_{OL} = 620μA, T_A = 25°C, V_{IA} ≤ 0.15V			0.55	V
Input Leakage Current	I_{OE}	OE = V_{CCA} or GND, V_{CCA} = 1.2V to 5.5V, V_{CCB} = 1.65V to 5.5V			±1	μA
High Impendence Output Leakage Current	I_{OZ}	Port A or Port B, OE = GND, V_{CCA} = 1.2V to 5.5V, V_{CCB} = 1.65V to 5.5V		±1	±2	μA
V_{CCA} Quiescent Current	I_{CCA}	V_I = V_{CCI} or GND, V_O = Open, I_O = 0			5	μA
V_{CCB} Quiescent Current	I_{CCB}	V_I = V_{CCI} or GND, V_O = Open, I_O = 0			5	μA
Combined Quiescent Current	I_{CCA}+I_{CCB}	V_I = V_{CCI} or GND, V_O = Open, I_O = 0			10	μA
High Impendence V_{CCA} Supply Current	I_{CCZA}	V_I = V_O = Open, I_O = 0, OE = GND			5	μA
High Impendence V_{CCB} Supply Current	I_{CCZB}	V_I = V_O = Open, I_O = 0, OE = GND			5	μA
OE Input Capacitance	C_I	V_{CCA} = 1.2V to 5.5V, V_{CCB} = 1.65V to 5.5V		3		pF
Port Capacitance	C_{IO}	V_{CCA} = 1.2V to 5.5V, V_{CCB} = 1.65V to 5.5V		5		pF
Resistor of NMOS between A port and B port	R_{PASS}	OE is logic high, I = 10mA, VI = 0.15V, V_{CCA} = 1.8V, V_{CCB} = 3.3V		500		Ω

4 Timing Requirements

Condition: T_A = 25°C, unless otherwise noted.

Parameter		Symbol	V_{CCB} = 1.8V	V_{CCB} = 2.5V	V_{CCB} = 3.3V	V_{CCB} = 5V	Unit
V_{CCA} = 1.2V							
			TYP.	**TYP.**	**TYP.**	**TYP.**	
Data Rate	Push-Pull		40	40	40	40	Mbps
	OD		2	2	2	2	
Pulse Duration	Push-Pull	t_W	25	25	25	25	ns
	OD		500	500	500	500	
V_{CCA} = 1.5V							
Data Rate	Push-Pull		80	80	80	80	Mbps
	OD		2	2	2	2	
Pulse Duration	Push-Pull	t_W	12.5	12.5	12.5	12.5	ns
	OD		500	500	500	500	
V_{CCA} = 1.8V							
			Min.	**Min.**	**Min.**	**Min.**	
Data Rate	Push-Pull		80	100	100	100	Mbps
	OD		2	2	2	2	
Pulse Duration	Push-Pull	t_W	12.5	10	10	10	ns
	OD		500	500	500	500	
V_{CCA} = 2.5V							
Data Rate	Push-Pull		-	100	100	100	Mbps

Parameter		Symbol	V_{CCB} = 1.8V	V_{CCB} = 2.5V	V_{CCB} = 3.3V	V_{CCB} = 5V	Unit
	OD		-	2	2	2	
Pulse Duration	Push-Pull	tw	-	10	10	10	ns
	OD		-	500	500	500	
V_{CCA} = 3.3V							
Data Rate	Push-Pull		-	-	100	100	Mbps
	OD		-	-	2	2	
Pulse Duration	Push-Pull	tw	-	-	10	10	ns
	OD		-	-	500	500	
V_{CCA} = 5V							
Data Rate	Push-Pull		-	-	-	100	Mbps
	OD		-	-	-	2	
Pulse Duration	Push-Pull	tw	-	-	-	10	ns
	OD		-	-	-	500	

5 Parameter Measurement Circuit

5.1 Waveform

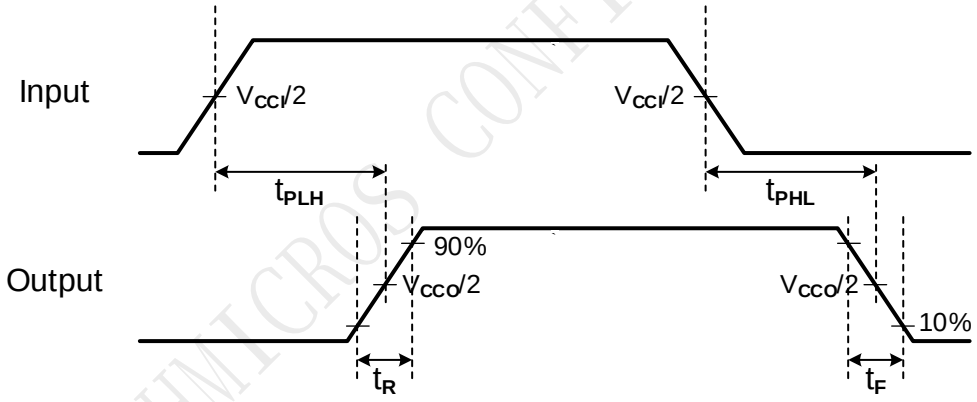


Figure 4. Propagation Delay, rising time, falling time

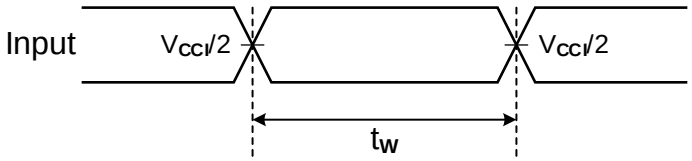


Figure 5.Pulse Duration (Push-Pull)

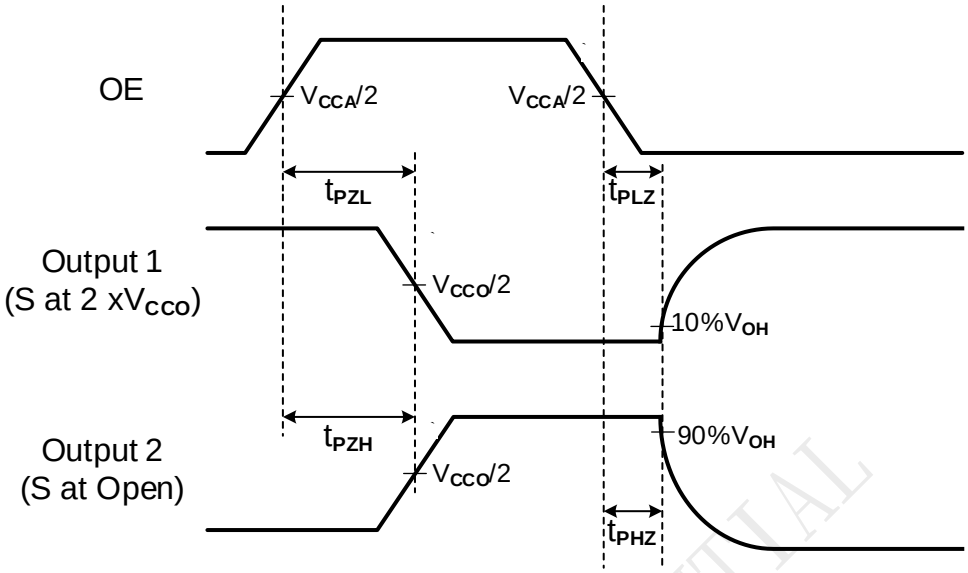


Figure 6. Enable and Disable Time

Output 1 waveform is for an output with internal that the output is high except when OE=1.

Output 2 waveform is for an output with internal that the output is low except when OE=0.

5.2 Load Circuit

Figure 10 shows the push-pull driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time. Figure 11 shows the open-drain driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time.

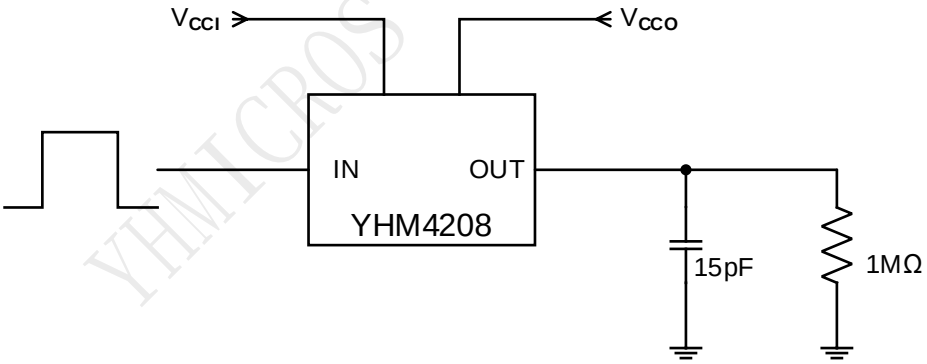


Figure 7. Push-Pull Input Load Circuit

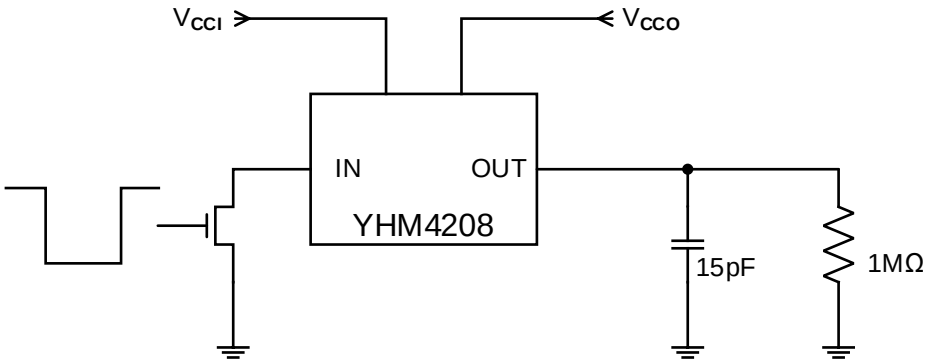


Figure 8. Open Drain Load Circuit

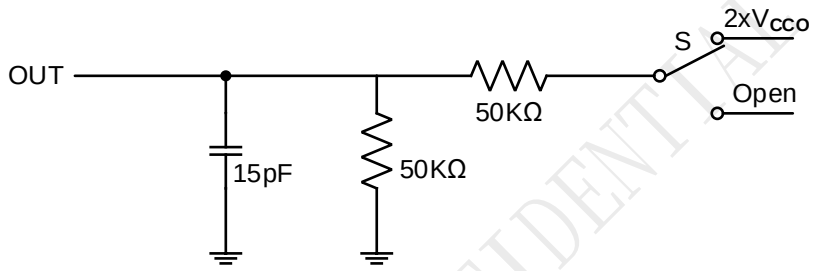


Figure 9. Load Circuit for Enable Time and Disable Time Measurement

Test	S
t_{PZL}, t_{PLZ} (t_{DIS})	2 x Vcco
t_{PZH}, t_{PHZ} (t_{EN})	Open

6 Typical Operating Characteristics

TBD

7 Detailed Description

7.1 General Introduction

The YHM4208 is an auto-direction voltage level translator which designed for translating logic voltage levels. The port A support voltage range from 1.2V to 5.5V and port B support voltage range from 1.65 to 5.5V. The device uses pass gate architecture with edge accelerator to improve the data rate. The pull up resistors have been integrated for open drain applications and external resistor is not needs. The device can translate push-pull CMOS logic outputs and open drain outputs.

7.2 Feature Description

7.2.1 Architecture

Figure 13 describes YHM4208 one cell architecture design. This application requires for both push-pull and open drain mode. This application uses edge-rate accelerator circuitry, a high-on-resistance N-channel pass-gate transistor and pull-up resistors to meet these requirements. This design needs no direction control signal. The resulting implementation supports both low-speed open-drain operation as well as high-speed push-pull operation.

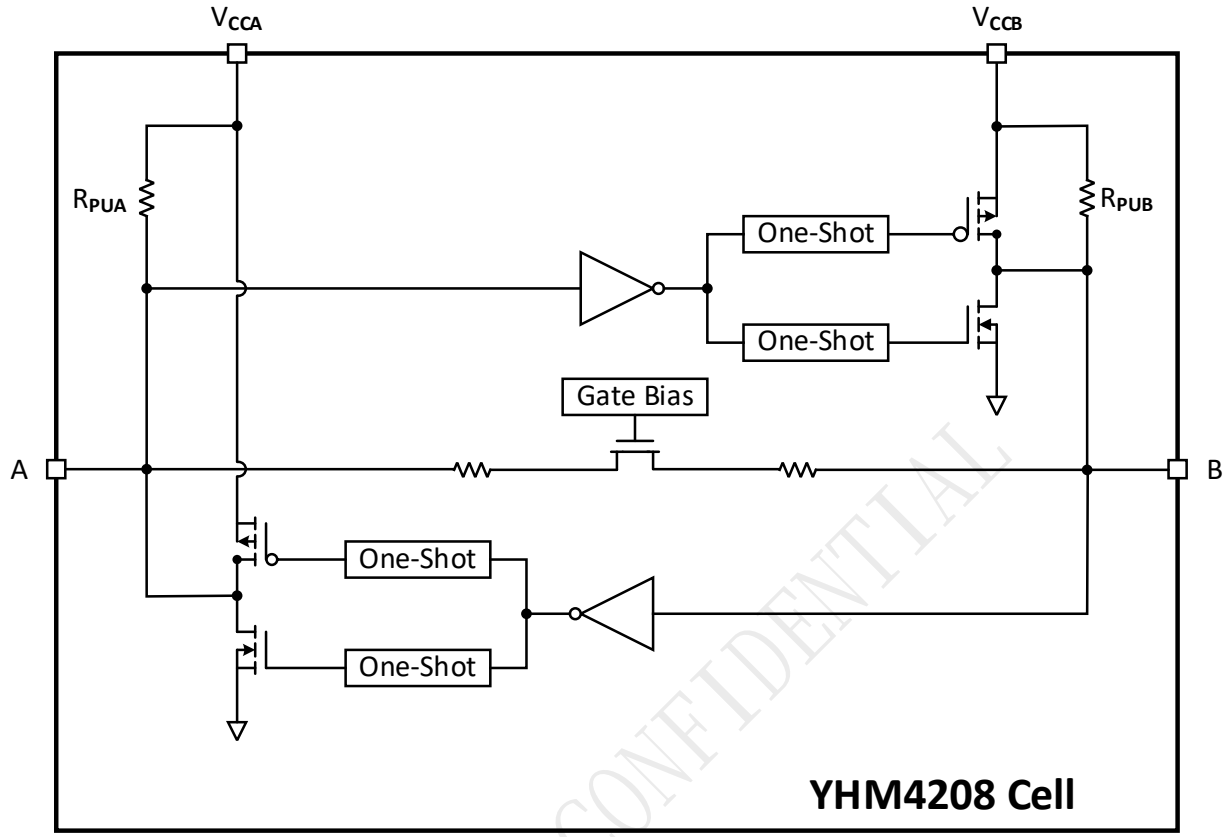


Figure 10. YHM4208 Cell Architecture

When transmitting data from A ports to B ports, during a rising edge the one-shot circuit turns on the PMOS transistor for a short-duration which reduces the low-to-high transition time. During a falling edge, the one-shot circuit turns on the N-channel MOSFET transistor for a short-duration which speeds up the high-to-low transition. Similarly, when transmitting data from B ports to A ports, during a rising edge the one-shot circuit turns on the PMOS transistor for a short-duration which reduces the low-to-high transition time. During a falling edge, the one-shot circuit turns on NMOS transistor for a short-duration and speeds up the high-to-low transition.

7.2.2 Input Driver Requirements

The fall time (t_F) of a signal depends on the edge-rate and output impedance of the external device driving YHM4208 data I/Os, as well as the capacitive loading on the data lines. Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_F, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω.

7.2.3 Output Load Considerations

Careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one-shot triggering takes place. PCB signal trace-lengths should be kept short enough so that the round trip delay is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The one-shot circuits have been designed to stay on for approximately 50 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The one-shot duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance of the YHM4208 output.

7.2.4 Enable and Disable

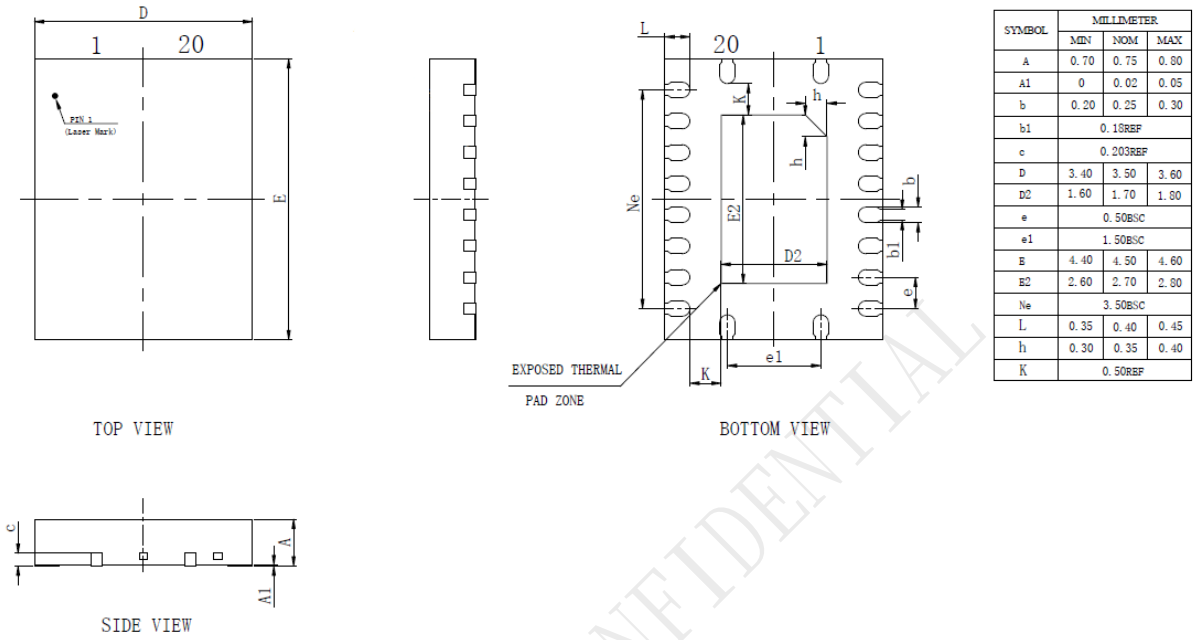
The YHM4208 has an OE pin input that is used to disable the device by setting the OE pin low, which places all I/Os in the Hi-Z state. The disabled time (t_{DIS}) indicates the delay between the time when the OE pin goes low and when the outputs get disabled (Hi-Z). The enable time (t_{EN}) indicates the amount of time the design must allow for the one-shot circuitry to become operational after the OE pin goes high.

7.2.5 Pull-up or Pull-down Resistors on I/O Lines

The YHM4208 has the smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40KΩ when the output is driving low. R_{PUA} and R_{PUB} have a value of 4KΩ when the output is driving high. R_{PUA} and R_{PUB} are disabled when OE = Low. This feature provides lower static power consumption and supports lower V_{OL} values for the same size pass-gate transistor and helps improve simultaneous switching performance.

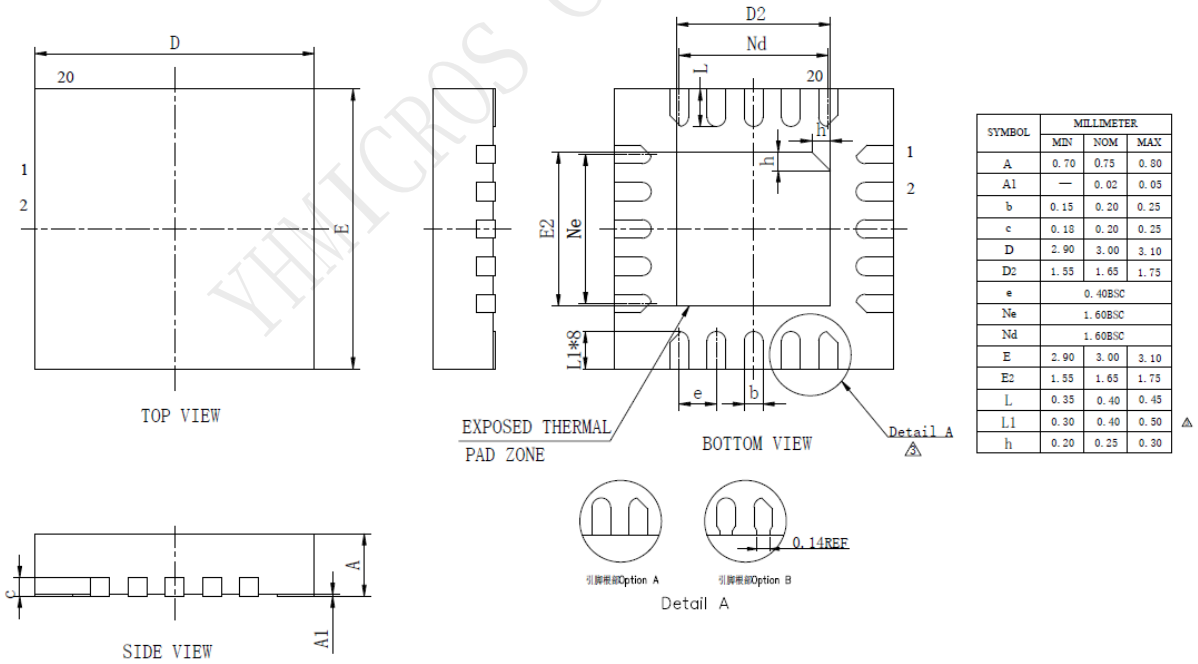
8 Package Dimensions

3.5mm x 4.5mm VQFN-20



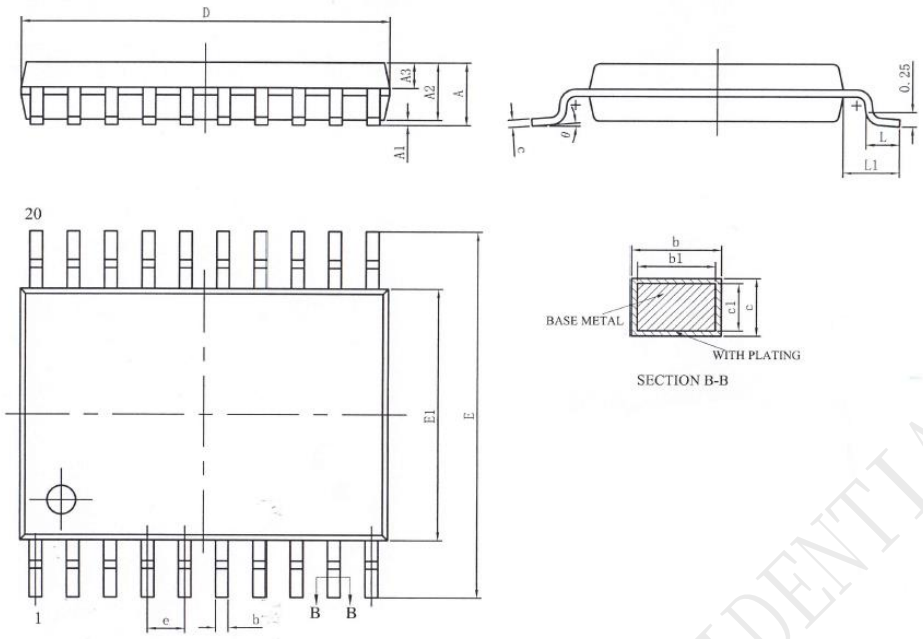
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.203REF	
D	3.40	3.50	3.60
D2	1.60	1.70	1.80
e		0.50BSC	
e1		1.50BSC	
E	4.40	4.50	4.60
E2	2.60	2.70	2.80
Ne		3.50BSC	
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K		0.50REF	

3mm x 3mm QFN-20



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e		0.40BSC	
Ne		1.60BSC	
Nd		1.60BSC	
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
L1	0.30	0.40	0.50
h	0.20	0.25	0.30

TSSOP-20



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

9 Ordering Information

Part Number	Package	Package Size	Top Mark (Note 1)	MOQ
YHM4208VQFT	20 VQFN	3.5mm x 4.5mm	YHM4208 YYWW xxxxxxx	3000
YHM4208QFT	20 QFN	3mm x 3mm	YHM4208 YYWW xxxxxxx	3000
YHM4208TFT	20 TSSOP	6.5mm x 4.4mm	YHM4208 YYWW xxxxxxx	4500

T = Tape and reel.

Note 1:

YY: Production year; WW: Production week.

xxxxxxx: Lot Number.

10 Datasheet Change History

Rev	Date	Changes
1.01	Feb/2024	Initial Version